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| EWULogo.png | | **EAST WEST UNIVERSITY** | | |
| **Department of Computer Science and Engineering** | | |
| **B.Sc. in Computer Science and Engineering Program** | | |
| **Mid Term I Examination, Fall2021, Makeup** | | |
| **Course:** | | **CSE360 – Computer Architecture, Section-3** | |  |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department** | |  |
| **Full Mark:** | | **25** | |  |
| **Time:** | | **1 Hour and 20 Minutes** | |  |
| **Note:** There are FIVE questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin. | | | | |
| 1. | The hypothetical machine has two instructions:  0100 = Load AC from I/O  0101 = Store AC to I/O  0110 = Add AC to Memory  In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:   1. Load AC from device 14 2. Add contents of memory location 940 3. Store AC to device 17   Assume that the next value retrieved from device 14 is 16 and that location 940 contains a value of 20 | | [CO1, C2, Mark: 6] | |
| 2. | Consider two microprocessors having 16- and 32-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.  a. Suppose all instructions and operands are four bytes long. If the number of instructions is 300, by what factor do the maximum data transfer rates differ?  b. Repeat assuming that half of the operands and instructions are two-byte long. | | [CO2, C3 Mark: 3+3] | |
| 3. | A microprocessor has an increment memory direct instruction, which adds 3 to the value in a memory location. The instruction has five stages: fetch opcode (2 bus clock cycle), fetch operand address (4 bus clock cycle), fetch operand (8 bus clock cycle), add 3 to operand (5 clock cycle), and store operand (7 clock cycle).   1. By what amount in percent will the duration of the instruction increase if we insert three bus wait states in each memory read and four bus wait states in memory write operations? 2. Repeat assuming that the increment operation taken 20 clock cycles instead of 5 clock cycles. | | [CO1, C2, Mark: 3+2] | |
| 4. | A CPU operates at a clock frequency of 125 GHz, requires an average of 77 CPI for executing one instruction, **what** is the performance (in MIPS) of the CPU? | | [CO1, C3,  Mark: 3] | |
| 5. | A 64-bit microprocessor, with a 64-bit external data bus is driven by an 64-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals six input clock cycles.   1. **What** is the maximum data transfer rate across the bus? 2. To increase its performance, would it be better to double the external clock frequency or to make its external data bus 128 bits supplied to the microprocessor? State any other assumptions you make and explain. | | [CO1, C3,  Mark: 2+ 3] | |